



# STP40N20 STW40N20

## N-CHANNEL 200V - 0.038Ω - 40A TO-220/TO-247 LOW GATE CHARGE STRipFET™ MOSFET

**Table 1: General Features**

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>	P <sub>w</sub>
STP40N20	200 V	< 0.045 Ω	40 A	160 W
STW40N20	200 V	< 0.045 Ω	40 A	160 W

- TYPICAL R<sub>DS(on)</sub> = 0.038 Ω
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATIBILITY
- EXCELLENT FIGURE OF MERIT (R<sub>DS</sub>\*Q<sub>g</sub>)
- 100% AVALANCHE TESTED

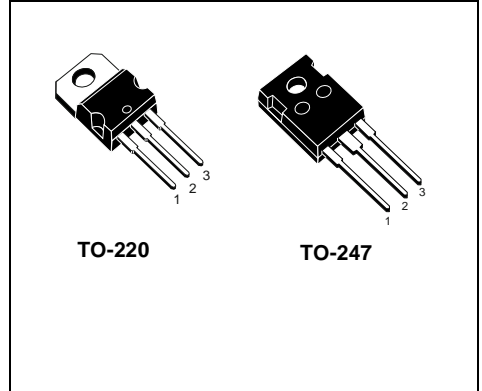
### DESCRIPTION

This MOSFET series realized with STMicroelectronics unique STRipFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency isolated DC-DC converters.

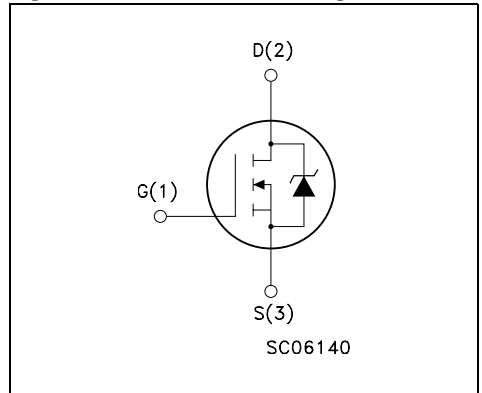
### APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- UPS

**Figure 1: Package**



**Figure 2: Internal Schematic Diagram**



**Table 2: Order Codes**

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP40N20	P40N20	TO-220	TUBE
STW40N20	W40N20	TO-247	TUBE

**Table 3: Absolute Maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source Voltage ( $V_{GS} = 0$ )	200	V
$V_{DGR}$	Drain-gate Voltage ( $R_{GS} = 20\text{ k}\Omega$ )	200	V
$V_{GS}$	Gate- source Voltage	$\pm 20$	V
$I_D$	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	40	A
$I_D$	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	25	A
$I_{DM}(\bullet)$	Drain Current (pulsed)	160	A
$P_{TOT}$	Total Dissipation at $T_C = 25^\circ\text{C}$	160	W
	Derating Factor	1.28	W/ $^\circ\text{C}$
$dv/dt(1)$	Peak Diode Recovery voltage slope	12	V/ns
$T_j$ $T_{stg}$	Operating Junction Temperature Storage Temperature	-55 to 150	$^\circ\text{C}$

(●) Pulse width limited by safe operating area

(1)  $I_{SD} \leq 40\text{A}$ ,  $di/dt \leq 200\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_j \leq T_{JMAX}$ .

**Table 4: Thermal Data**

		TO-220	TO-247	
Rthj-case	Thermal Resistance Junction-case Max	0.78		$^\circ\text{C}/\text{W}$
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	50	$^\circ\text{C}/\text{W}$
$T_j$	Maximum Lead Temperature For Soldering Purpose	300		$^\circ\text{C}$

**Table 5: Avalanche Characteristics**

Symbol	Parameter	Max Value	Unit
$I_{AR}$	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by $T_j$ max)	40	A
$E_{AS}$	Single Pulse Avalanche Energy (starting $T_j = 25^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	230	mJ

**ELECTRICAL CHARACTERISTICS** ( $T_{CASE} = 25^{\circ}C$  UNLESS OTHERWISE SPECIFIED)**Table 6: On/Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 1mA, V_{GS} = 0$	200			V
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}, T_C = 125^{\circ}C$			1 10	$\mu A$ $\mu A$
$I_{GSS}$	Gate-body Leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20V$			$\pm 100$	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10V, I_D = 20 A$		0.038	0.045	$\Omega$

**Table 7: Dynamic**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (1)$	Forward Transconductance	$V_{DS} = 15 V, I_D = 20 A$		30		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25V, f = 1 \text{ MHz}, V_{GS} = 0$		2500 510 78		pF pF pF
$t_{d(on)}$ $t_r$ $t_{d(off)}$ $t_f$	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	$V_{DD} = 100 V, I_D = 20 A,$ $R_G = 4.7 \Omega, V_{GS} = 10 V$ (Resistive Load see, Figure 17)		20 44 74 22		ns ns ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 160V, I_D = 40 A,$ $V_{GS} = 10V$		75 13.2 35.5		nC nC nC

**Table 8: Source Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM} (2)$	Source-drain Current Source-drain Current (pulsed)				40 160	A A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 20 A, V_{GS} = 0$			1.5	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 20 A, di/dt = 100A/\mu s$ $V_{DD} = 100V, T_j = 25^{\circ}C$ (see test circuit, Figure 18)		192 922 9.6		ns nC A
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 20 A, di/dt = 100A/\mu s$ $V_{DD} = 100V, T_j = 150^{\circ}C$ (see test circuit, Figure 18)		242 1440 11.9		ns nC A

(1) Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %.

(2) Pulse width limited by safe operating area.

Figure 3: Safe Operating Area For TO-220

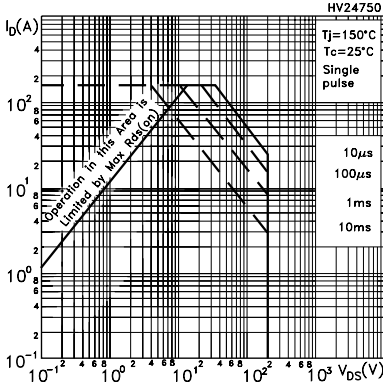


Figure 4: Safe Operating Area For TO-247

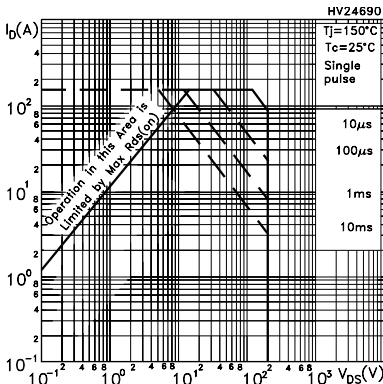


Figure 5: Output Characteristics

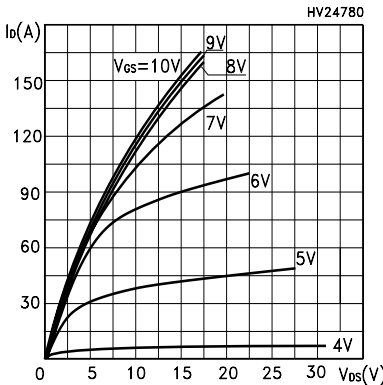


Figure 6: Thermal Impedance For TO-220

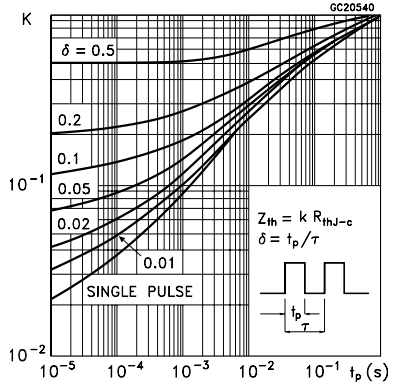


Figure 7: Thermal Impedance For TO-247

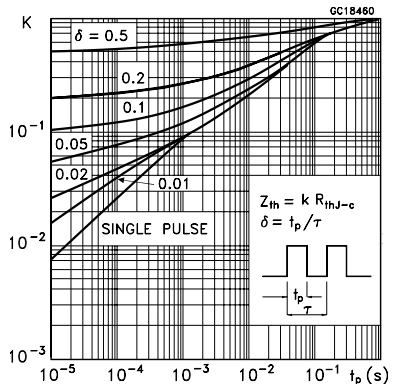


Figure 8: Transfer Characteristics

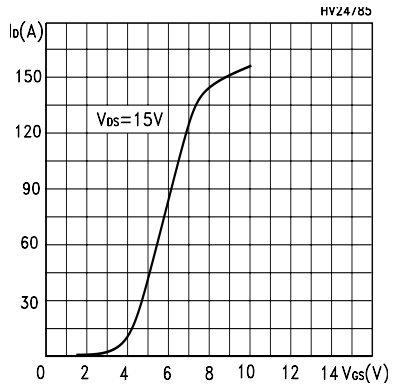


Figure 9: Transconductance

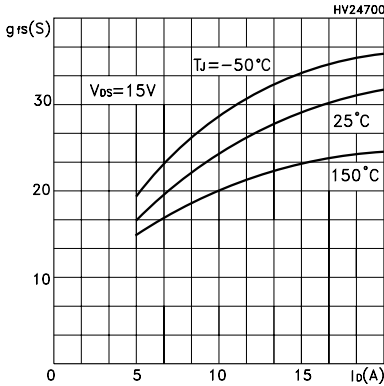


Figure 10: Gate Charge vs Gate-source Voltage

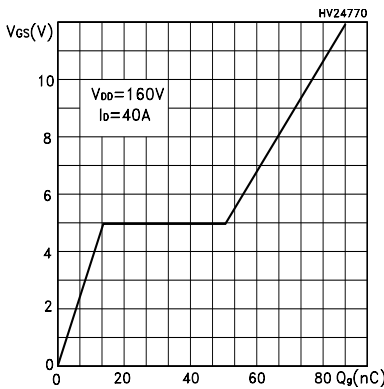


Figure 11: Normalized Gate Threshold Voltage vs Temperature

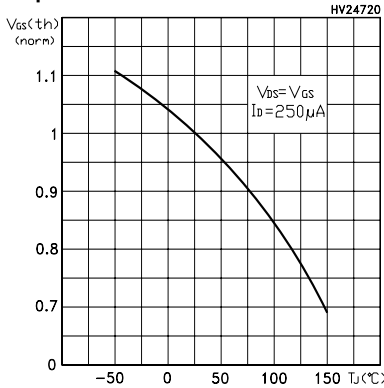


Figure 12: Static Drain-source On Resistance

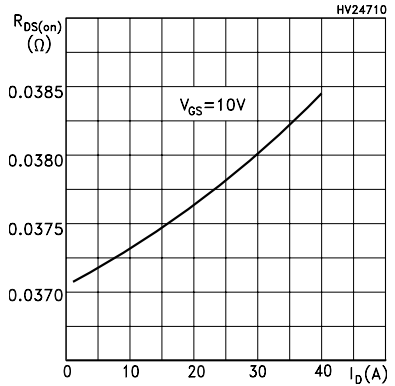


Figure 13: Capacitance Variations

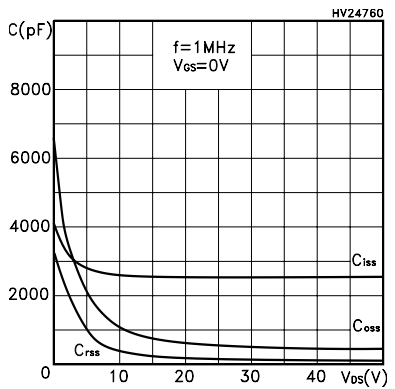
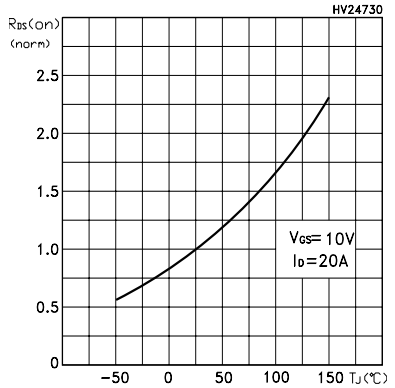


Figure 14: Normalized On Resistance vs Temperature



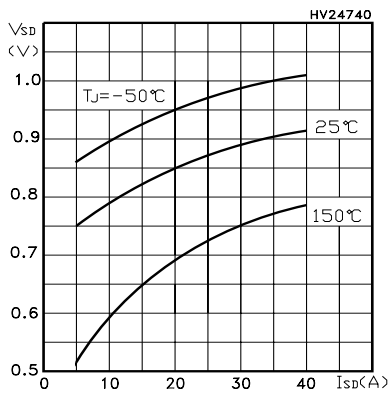
**Figure 15: Source-Drain Forward Characteristics**

Figure 16: Unclamped Inductive Load Test Circuit

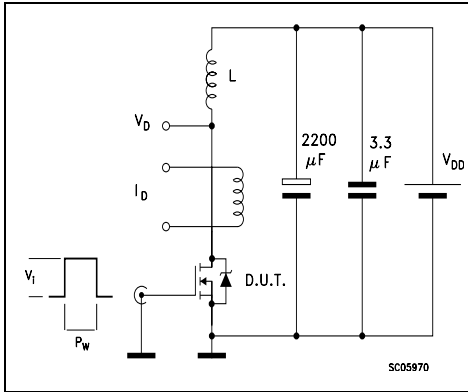


Figure 17: Switching Times Test Circuit For Resistive Load

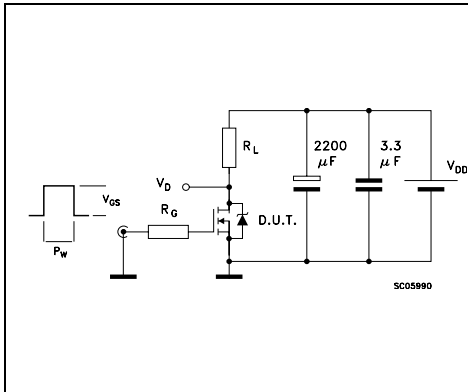


Figure 18: Test Circuit For Inductive Load Switching and Diode Recovery Times

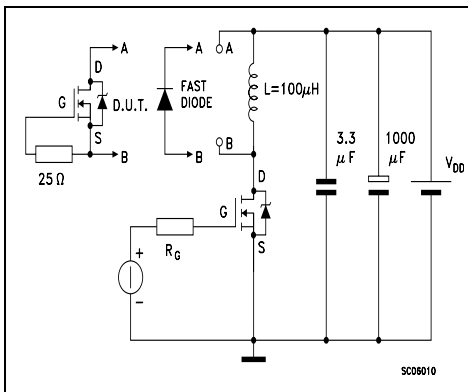


Figure 19: Unclamped Inductive Wavform

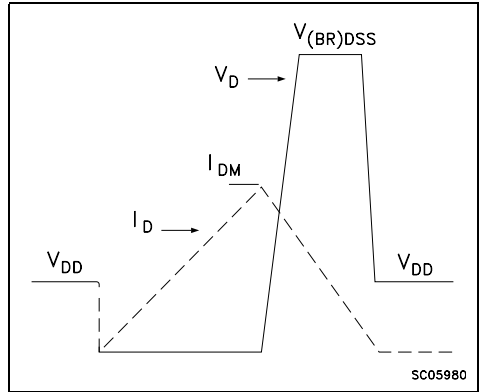


Figure 20: Gate Charge Test Circuit

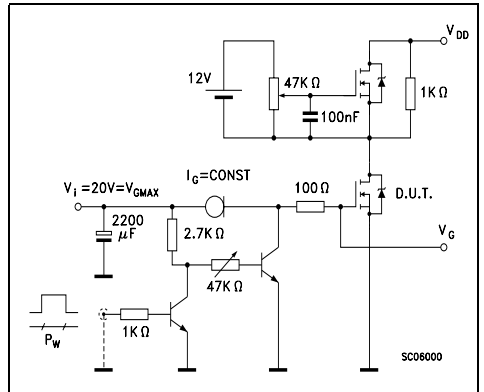


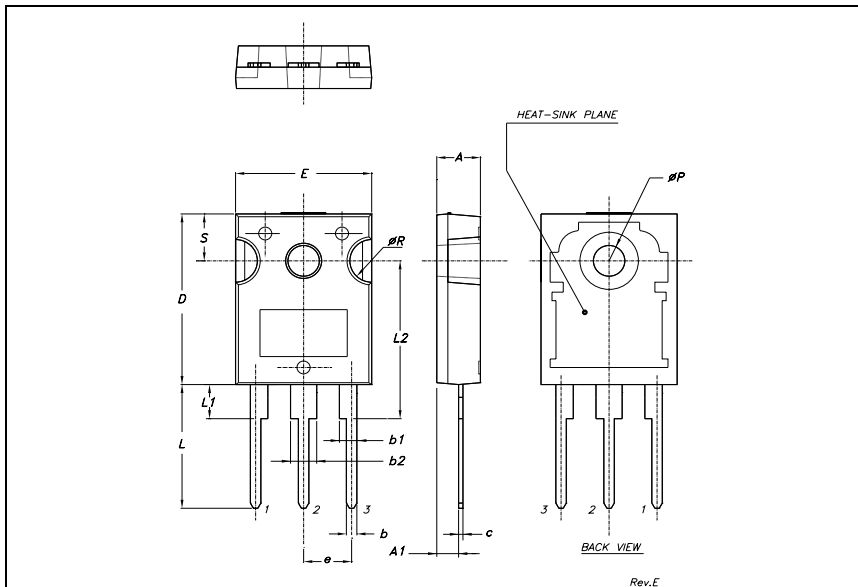
Figure 18: Test Circuit For Inductive Load Switching and Diode Recovery Times





## TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



**Table 9: Revision History**

<b>Date</b>	<b>Revision</b>	<b>Description of Changes</b>
27-Sep-2004	1	First Release.
03-Feb-2005	2	Complete Version

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